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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
(213.003-D2-US)

In re Application of: **Ye et al.**

Serial No: **10/763,142**

Filed: **January 22, 2004**

Title: **Method and Apparatus for Monitoring  
Integrated Circuit Fabrication**

) Group Art Unit: **2125**

) Examiner:

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**STATEMENT OF RELATED APPLICATIONS**

Dear Sir:

The above-referenced application is related to the following applications which all claim priority to "Method and Apparatus for Monitoring Integrated Circuit Fabrication", Serial No. 10/677,563, filed October 2, 2003:

1. "Method and Apparatus for Monitoring Integrated Circuit Fabrication",  
Serial No. 10/756,718, filed January 13, 2004 (still pending); and
2. "Method and Apparatus for Monitoring Integrated Circuit Fabrication",  
Serial No. 10/763,433, filed January 23, 2004 (still pending).

Date: May 17, 2004

Respectfully submitted,

Neil A. Steinberg  
Reg. No. 34,735  
650-968-8079



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**Certificate of Mailing under 37 CFR 1.8**

I hereby certify that the attached Statement of Related Applications (1 page) is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

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